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Abstract
The representation of audio, image and video signals involves a vast amount of data, so signal compression is indispensable. Recently, variable length code (VLC) has been widely used in multimedia and lossless coding compression such as JPEG and MPEG. This thesis describes an efficient class-based VLC encoder/decoder and its VLSI architecture for MPEG-4. It takes advantage of logic optimization techniques, and achieves high throughput. The computation complexity of the proposed VLC is quite low and its memory requirement is small. Hence, it is easily implemented by VLSI and very suitable for real-time MPEG-4 applications.

The VLC architecture has been synthesized on Synopsys Design Compiler with the standard-cell from TSMC 0.35-μm cell library. Finally, the layout for the design was generated with the Avant! tools, Apollo (for floorplan, placement and routing). The gate counts and core size of VLC encoder/decoder are 9624/9486 and / , respectively. In the simulation, it’s clock frequency achieves 50MHz.
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